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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,532	10/28/2003	Sun Hyoung Lee	DAE-0011	6426

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,532	LEE ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-14* is/are rejected.

7)☒ Claim(s) *8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings received on 28 October 2003 are deemed acceptable.

Claim Objections

3. Claims 1-14 are objected to because of the following informalities:

Acronyms (such as SRAM and DRAM in claim 1) should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. An acceptable correction would be for example in claim 1, "Dynamic Random Access Memory (DRAM) cells".

As for claim 8, the phrase "DRAM calls" in line four of this claim should be changed to "DRAM cells".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. (hereinafter Leung) US Patent 5,999,474.

As for claim 12, Leung teaches a method of driving an SRAM-compatible memory having a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory interfacing with an external system in which no timing period is externally set for a refresh operation of the DRAM cells, comprising (referring to Fig. 1, the DRAM is divided into 64 unique memory banks (elements 0-63). Each memory bank is a matrix of rows and columns – col. 4, lines 45-53. The DRAM are SRAM compatible as described in col. 4, lines 13-20):

providing multiple pieces of input data to the memory banks, each piece of the input data being provided to corresponding one of the memory banks (col. 2, lines 34-43 – data can be written to any of the memory banks);

determining whether a refresh operation or a write operation for a previous frame is being performed in the memory banks (col. 10, lines 20-35 – read/write operations are mutually exclusive as to provide the write command with priority over the refresh command. This way Leung's system can make the determination and prioritize which operation is currently being performed on the DRAM bank).

storing a piece of the input data in a data buffer if the refresh operation or the write operation is being performed in a certain memory bank,

wherein the piece of the input data is provided to the certain memory bank and write operation of the piece of the input data is suspended (col. 7, lines 1-7, the write data is written to the cache/buffers rather than directly to the memory bank. During this write hit access the memory banks access is suspended as the refresh operation takes place in the memory bank – col. 7, liens 60-65); and

writing the piece of the input data stored in the data buffer into DRAM cells of the certain memory bank after the refresh operation or the write operation is completed (again in col. 10, lines 20-35, the write request signal is used to assert the write operation into the DRAM. Once the determination is made that write access is granted, the data now stored in the cache can be destaged to the DRAM bank);

wherein the memory banks except for the certain memory bank independently perform write operations, while the refresh operation or the write operation for the previous frame is performed with respect to the certain memory bank. Col. 2, lines 34-43 indicate that read write and refresh operations can be independently controlled within each bank. Data is first written to a write buffer, then written to one of the respective memory banks. The abstract of Leung's teachings further indicate that the DRAM banks are operated with independent control, enabling parallel refresh operations and read-write access to different banks. As an example, Leung teaches in lines 55-61 of col. 4 that one DRAM bank can be accessed (i.e. written) while another of the other remaining banks may be written to.

As for claim 14, Leung teaches storing an input address designating DRAM cells in the certain memory bank into and address buffer (col. 7, lines 5-13 – the address buffer (element 181) stores the address, which identifies the bank, row and column number to be accessed); and

providing the input address to the certain memory bank after the refresh or write operation is completed (The read/write and refresh signals are mutually exclusive which prevents the data and addresses to be sent from the buffers to the banks until the DRAM bank previous operations (i.e. read/write) are complete – col. 10, lines 20-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-6, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung and in further view of Fujioka et al. (hereinafter Fujioka) US PG Publication 2003/0106010.

As for claim 1, Leung teaches An SRAM-compatible memory having a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory interfacing with an external system in which no timing period is externally set for

a refresh operation of the DRAM cells, comprising (referring to Fig. 1, the DRAM is divided into 64 unique memory banks (elements 0-63). Each memory bank is a matrix of rows and columns – col. 4, lines 45-53. The DRAM are SRAM compatible as described in col. 4, lines 13-20):

the plurality of memory banks for storing input data in DRAM cells specified by an input address externally provided (col. 5, lines 12-16 – the external device asserts an address signal to provide the address to a address decoder), wherein write operations of the memory banks are independently controlled such that when a refresh operation or a write operation for a previous frame is being performed in a certain memory bank, write operation of input data is independently performed with respect to the respective memory banks except for the certain memory bank (col. 2, lines 34-43 indicate that read write and refresh operations can be independently controlled within each bank. Data is first written to a write buffer, and then written to one of the respective memory banks. The abstract of Leung's teachings further indicate that the DRAM banks are operated with independent control, enabling parallel refresh operations and read-write access to different banks. As an example, Leung teaches in lines 55-61 of col. 4 that one DRAM bank can be accessed while one of the remaining banks may be written to);

Leung however teaches neither a parity generator, nor a parity bank used to store the generated parity data.

Fujioka however teaches a memory circuit having a parity cell array in which he includes a parity generator for generating an input parity based on the

input data (paragraph 0033, lines 3-6 – Fujioka teaches a parity generating circuit which generates parity data for write data (i.e. input data)), the input parity having a certain preset parity value in conjunction with the input data (paragraph 0035 through paragraph 0036 line 3 teaches the generated parity data as being written to a parity cell array. Further a test judgment circuit receives read out data from cell arrays and parity data from the parity cell array and compares the results – paragraph 0038, lines 1-4. In other words, the parity data has a preset value as it is already established and stored in the parity cell array prior to its comparison by the judgment circuit); and

a parity bank for storing the input parity (the parity data is written to the parity cell array (i.e. bank) – paragraph 0035, lines 1-5).

As for claim 2, Leung teaches The SRAM-compatible memory as set forth in claim 1, further comprising:

a plurality of bank control units for controlling the refresh operation and the write operation of the memory banks, each of the bank control units being associated with corresponding one of the memory banks (Fig. 3 depicts one of the access control units as illustrated in Fig. 1 (element 100 for example) which are associated with each of the 64 banks. Referring to Fig. 3, the control unit contains row and column decoders used for write operations (elements 205 and 206 respectively and refreshing logic (i.e. element 208, refresh counter) – col. 9, lines 19-38)); and

Fujioka additionally teaches what Leung fails to teach which includes a parity control unit for controlling the refresh operation and the write

operation of the parity bank (since the parity cell array (PCA) as described by Fujioka is a DRAM – paragraph 0019, lines 1-2 it is inherent that the PCA has control logic for writing to, and refreshing the cells. Referring to Fig. 11, Fujioka teaches a control unit, which is comprised of the refresh generating circuit (element 32) and shift register circuit (element 36) which are used to refresh the cells, and select memory block respectively – paragraph 0069, lines 1-9; and paragraph 0070, lines 1-7).

As for claim 5, Leung teaches the SRAM-compatible memory as set forth in claim 2, further comprising a refresh address generator for generating a refresh address to designate DRAM cells of the memory banks to be refreshed (col. 11, lines 29-30).

As for claim 6, Leung teaches the SRAM-compatible memory as set forth in claim 5, wherein each of the bank control units further comprises an address selector for selecting one of the input address and the refresh address and providing the selected address to corresponding one of the memory banks to perform the write operation or the refresh operation with respect to DRAM cells in the corresponding one of the memory banks (referring again to Fig. 11, the row and column decoders (elements 205 and 206 respectively) are contained in each of the control units which are used to control addresses for write and refresh operations (col. 11, lines 7-28)).

As for claim 11, Leung teaches the SRAM-compatible memory as set forth in claim 2, wherein the parity bank has a substantially same structure as each of the memory banks (referring to Fig. 11, the PCA memory is defined

by multiple banks, each containing rows and columns of cells – paragraph 0106 – lines 1-8).

As for claim 13, though Leung fails to teach the limitations of this claim, Fujioka teaches obtaining an input parity from a predetermined preset parity value and the input data and writing the input parity into a parity bank (paragraph 0035 through paragraph 0036 line 3 teaches the generated parity data as being written to a parity cell array. Further a test judgment circuit receives read out data from cell arrays and parity data from the parity cell array and compares the results – paragraph 0038, lines 1-4. In other words, the parity data has a preset value as it is already established and stored in the parity cell array prior to its comparison by the judgment circuit).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Leung to further include Fujioka's parity circuit in his own system. By doing so, Leung would benefit by having a system for his SRAM-compatible DRAM which includes ECC and BIST testing which would not only allow for self correcting of errors inherit in memory cells as densely packed as 1T-cells, but also allow for reduced test time of his memory as taught by Fujioka (paragraph 0022, lines 1-4).

6. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Leung and Fujioka, and in further view of MacLaren et al. (hereinafter MacLaren) US PG Publication 2002/0016942 A1.

As for claim 3, Leung teaches an SRAM-compatible memory which includes:

a data buffer for storing input data whose write operation in a memory bank is suspended due to a refresh operation or a write operation for a previous frame in the memory bank (the buffer/cache unit (comprised of the SRAM cache, and read/write buffers (elements 187, 188-9 respectively)), will store the write data to be written to the bank before it's written to the bank – col. 7, lines 42-47. By doing so, the DRAM bank that is selected to receive the data can be refreshed during this write hit access. Once the refresh is complete the data can be destaged into the data bank – col. 7, lines 60-65); and

an address buffer for storing input address designating DRAM cells of the memory bank (col. 7, lines 5-13 – the address buffer (element 181) stores the address which identifies the bank, row and column number to be accessed).

Leung however does not teach containing both of said buffers in the same control unit as claimed by applicant. MacLaren teaches a system for error detection, which includes a host controller, which can contain one or more memory controller devices, which in turn contains data and address buffers (paragraph 0021, lines 1-15). Referring to Fig. 3, in one embodiment, each memory controller device is associated with unique blocks of memory.

It would have been obvious to one of ordinary skill in art at the time of the invention for Leung include the data and address buffers in each of the control units as similarly taught by MacLaren. By doing so, Leung would benefit by

storing buffered address data adjacent to each of the memory banks which in turn would improve his system in recovering from soft errors more quickly, hence correcting errors before system a more critical system failure can occur as taught by MacLaren in paragraph 007, lines 23-27.

As for claim 4, Leung teaches providing data from the buffer to the memory bank after the refresh or write operation is completed, and the address buffer provides input address to the memory bank after the refresh or write operation is compete. Referring again to col. 7, lines 1-7, the write data is written to the cache/buffers rather than directly to the memory bank. Likewise, col. 7, lines 5-13 – the address buffer (element 181) stores the address, which identifies the bank, row and column number to be accessed. During the write hit access, the memory bank access is suspended as the refresh operation takes place in the memory bank – col. 7, lines 60-65. Furthermore, the read/write and refresh signals are mutually exclusive which prevents the data and addresses to be sent from the buffers to the banks until the DRAM bank previous operations (i.e. read/write) are complete – col. 10, lines 20-35.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Leung and Fujioka, and in further view of Tsukude US PG Publication 2003/0185078 A1.

As for claim 7, though Leung teaches his bank control units as controlling the refresh operation of each memory bank (referring again to Fig. 3, the refresh circuitry is contained with the control unit – col. 11, lines

7-20), he fails to teach his SRAM-compatible memory as comprising a flag generator for generating a refresh flag signal to the bank control units.

Tsukude however teaches a semiconductor memory device which aims at improving the refresh function of a DRAM memory device. In his disclosure, Tsukude teaches a flag generator for generating a refresh flag signal to the control unit (paragraph 0045, lines 1-14 – the refresh flag generator (100) generates a request for a refresh operation to the refresh controller (400)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Leung to further utilize Tsukude's memory device with refresh flag generating circuit. By doing so, Leung would benefit by further being able to synchronize the read/write and refresh operations of his DRAM by alerting the control unit to assert the refreshing of the cells. Such synchronization could then prevent DRAM malfunction as taught by Tsukude in paragraph 009, lines 1-12.

Allowable Subject Matter

8. Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

As for claim 8, though the combined teachings of Leung, Fujioka and Tsukude teach using a flag generator to produce a refresh flag signal, they fail to teach or suggest the flag generator as being periodically activated, used specifically to control a refresh address generator, which generates an address to designate DRAM cells to be refreshed as claimed aimed by applicant.

Claims 9-10 further limit claim 8 therefore they too are deemed allowable.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lu et al. (US Patent 6,757,784 B2) teaches a system for hiding memory refreshing.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

REGINALD G. BRAGDON
PRIMARY EXAMINER